

## CLAIMS

1. An integrated circuit comprising:

a first node;

a second node;

a resistor coupling together the first and second nodes;

a comparator having two inputs and an output, a first one of the two inputs coupled to the resistor and the first node; and

a three-terminal device having a first terminal coupled to the second node and the resistor and having a second terminal coupled to the output of the comparator.

2. The integrated circuit of claim 1 wherein:

a second one of the two inputs of the comparator coupled to a first substantially constant voltage; and

a third terminal of the three-terminal device coupled to a second substantially constant voltage.

3. The integrated circuit of claim 2 wherein:

the first substantially constant voltage is provided by a voltage supply; and

the second substantially constant voltage is a ground potential.

1 4. The integrated circuit of claim 2 wherein:

2 the three-terminal device is a MOSFET;

3 the first terminal of the three-terminal device is a drain electrode of the MOSFET;

4 the second terminal of the three-terminal device is a gate electrode of the MOSFET; and

5 the third terminal of the three-terminal device is a source electrode of the MOSFET.

1 5. The integrated circuit of claim 1 wherein:

2 the three-terminal device is a MOSFET;

3 the first terminal of the three-terminal device is a drain electrode of the MOSFET; and

4 the second terminal of the three-terminal device is a gate electrode of the MOSFET.

1 6. The integrated circuit of claim 1 wherein:

2 a magnitude of a voltage at the second node is less than a magnitude of a voltage at a  
3 second one of the two inputs of the comparator.

1 7. The integrated circuit of claim 1 wherein:

2 the second terminal of the three-terminal device is a control electrode; and

3 the three-terminal device is turned on by the control electrode when a magnitude of a  
4 voltage at the first node is greater than a magnitude of a voltage at a second one of the two inputs  
5 of the comparator.

1           8. The integrated circuit of claim 1 wherein:

2           when a magnitude of a voltage at the first node is greater than a magnitude of a voltage at  
3 a second one of the two inputs of the comparator, the three-terminal device turns on to reduce a  
4 magnitude of a voltage at the second node to be less than or equal to the magnitude of the  
5 voltage at the second one of the two inputs of the comparator.

1           9. The integrated circuit of claim 1 further comprising:

2           an input signal coupled to the first node.

1           10. The integrated circuit of claim 9 further comprising:

2           a voltage-sensitive circuit coupled to the second node,

3           wherein:

4           the voltage-sensitive circuit processes the input signal.

1 11. An integrated circuit comprising:

2 a first circuit;

3 a first node; and

4 a second circuit coupling the first circuit to the first node;

5 wherein:

6 the first circuit operates off of a supply voltage; and

7 the second circuit detects a voltage magnitude of a signal at the first node and  
8 reduces the voltage magnitude of the signal to equal a voltage magnitude of the supply voltage  
9 before transmitting the signal to the first circuit.

1 12. The integrated circuit of claim 11 further comprising:

2 a second node; and

3 a third circuit coupling the first circuit to the second node;

4 wherein:

5 the third circuit detects a voltage magnitude of a different signal at the second  
6 node and reduces the voltage magnitude of the different signal to equal a voltage magnitude of  
7 the supply voltage before transmitting the different signal to the first circuit.

1 13. An integrated circuit comprising:

2 a first node;

3 a second node;

4 a first resistor coupling together the first and second nodes;

5 a first three-terminal device being of a first type, a first terminal of the first three-terminal  
6 device coupled to the first resistor and the first node;

7 a second three-terminal device being of the first type, a first terminal of the second three-  
8 terminal device coupled to a first substantially constant voltage, a second terminal of the second  
9 three-terminal device coupled to a second terminal of the first three-terminal device and to a  
10 third terminal of the second three-terminal device;

11 a third three-terminal device being of a second type, a first terminal of the third three-  
12 terminal device coupled to a second substantially constant voltage, a third terminal of the third  
13 three-terminal device coupled to a third terminal of the first three-terminal device;

14 a fourth three-terminal device being of the second type, a first terminal of the fourth  
15 three-terminal device coupled to the second substantially constant voltage, a second terminal of  
16 the fourth three-terminal device coupled to a second terminal of the third three-terminal device  
17 and to a third terminal of the fourth three-terminal device;

18 a fifth three-terminal device being of the second type, a first terminal of the fifth three-  
19 terminal device coupled to the second substantially constant voltage, a second terminal of the  
20 fifth three-terminal device coupled to the third terminals of the first and third three-terminal  
21 devices, a third terminal of the fifth three-terminal device coupled to the first resistor and to the  
22 second node;

23 a sixth three-terminal device being of the first type, a first terminal of the sixth three-  
24 terminal device coupled to the third terminals of the first and third three-terminal devices and to  
25 the second terminal of the fifth three-terminal device, a second terminal of the sixth three-  
26 terminal device coupled to the first substantially constant voltage, a third terminal of the sixth  
27 three-terminal device coupled to the second terminals of the third and fourth three-terminal  
28 devices and to the third terminal of the fourth three-terminal device; and

29 a second resistor coupling together the second terminals of the first and second three-  
30 terminal devices and the third terminal of the second three-terminal device to the second  
31 terminals of the third and fourth three-terminal devices and to the third terminals of the fourth  
32 and sixth three-terminal devices.

1 14. The integrated circuit of claim 13 wherein:

2 the first, second, third, fourth, fifth, and sixth three-terminal devices are MOSFETs.

1 15. The integrated circuit of claim 13 wherein:

2 the first, second, and sixth three-terminal devices are p-channel MOSFETs; and

3 the third, fourth, and fifth three-terminal devices are n-channel MOSFETs.

1 16. The integrated circuit of claim 15 wherein:

2 the first terminals of the first, second, third, fourth, fifth, and sixth three-terminal devices  
3 are source electrodes;

4 the second terminals of the first, second, third, fourth, fifth, and sixth three-terminal  
5 devices are gate electrodes; and



6 the third terminals of the first, second, third, fourth, fifth, and sixth three-terminal devices  
7 are drain electrodes.

1 17. The integrated circuit of claim 13 further comprising:  
2 a seventh three-terminal device, second and third terminals of the seventh three-terminal  
3 device coupled to the second terminal of the fifth three-terminal device, to the third terminals of  
4 the first and third three-terminal devices, and to the first terminal of the sixth three-terminal  
5 device.

1 18. The integrated circuit of claim 17 further comprising:  
2 an eighth three-terminal device, a first terminal of the eighth three-terminal device  
3 coupled to the second substantially constant voltage, second and third terminals of the eighth  
4 three-terminal device coupled to a first terminal of the seventh three-terminal device.

1 19. The integrated circuit of claim 13 further comprising:  
2 a third resistor coupling the first node and the first resistor to the first terminal of the first  
3 three-terminal device.

1           20. The integrated circuit of claim 19 further comprising:

2           a seventh three-terminal device, second and third terminals of the seventh three-terminal  
3 device coupled to the second terminal of the fifth three-terminal device, to the third terminals of  
4 the first and third three-terminal devices, and to the first terminal of the sixth three-terminal  
5 device; and

6           an eighth three-terminal device, a first terminal of the eighth three-terminal device  
7 coupled to the second substantially constant voltage, second and third terminals of the eighth  
8 three-terminal device coupled to a first terminal of the seventh three-terminal device.

1           21. The integrated circuit of claim 20 wherein:

2           the first, second, and sixth three-terminal devices are p-channel MOSFETs;

3           the third, fourth, and fifth three-terminal devices are n-channel MOSFETs;

4           the first terminals of the first, second, third, fourth, fifth, and sixth three-terminal devices  
5 are source electrodes;

6           the second terminals of the first, second, third, fourth, fifth, and sixth three-terminal  
7 devices are gate electrodes; and

8           the third terminals of the first, second, third, fourth, fifth, and sixth three-terminal devices  
9 are drain electrodes.



22. A method of operating an integrated circuit comprising:  
detecting a signal at a first node, the signal having a first voltage magnitude;  
comparing the first voltage magnitude to a reference voltage magnitude;  
if the first voltage magnitude is less than the reference voltage magnitude,  
transferring the signal with the first voltage magnitude to a second node; and  
if the first voltage magnitude is greater than the reference voltage magnitude,  
reducing the first voltage magnitude to a second voltage magnitude less than or  
equal to the reference voltage magnitude; and  
transferring the signal with the second voltage magnitude to the second node.

23. The method of claim 22 further comprising:  
providing a supply voltage for the integrated circuit; and  
providing a magnitude of the supply voltage for the reference voltage magnitude.

24. The method of claim 23 further comprising:  
providing the magnitude of the supply voltage equal to approximately zero.

25. The method of claim 23 further comprising:  
providing the magnitude of the supply voltage greater than zero.

26. The method of claim 23 further comprising:  
varying the magnitude of the supply voltage from zero to greater than zero.

1 27. The method of claim 22 wherein:

2 reducing the first voltage magnitude further comprises:

3 conducting a current across a resistor to reduce the first voltage magnitude to the  
4 second voltage magnitude.

1 28. The method of claim 27 wherein:

2 reducing the first voltage magnitude further comprises:

3 turning on a transistor to conduct the current across the resistor.

1 29. The method of claim 22 further comprising:

2 operating the integrated circuit in a suspend mode;

3 detecting a different signal at the first node, the different signal having a third voltage  
4 magnitude;

5 comparing the first voltage magnitude to a different reference voltage magnitude;

6 if the third voltage magnitude is less than the different reference voltage magnitude,

7 transferring the different signal with the third voltage magnitude to the second  
8 node; and

9 if the third voltage magnitude is greater than the different reference voltage magnitude,

10 reducing the first voltage magnitude to a fourth voltage magnitude less than or  
11 equal to the different reference voltage magnitude; and

12 transferring the different signal with the fourth voltage magnitude to the second  
13 node.

30. The method of claim 22 further comprising:  
operating the integrated circuit in a suspend mode;  
detecting a different signal at the first node, the different signal having a third voltage  
magnitude;  
comparing the first voltage magnitude to a different reference voltage magnitude;  
if the third voltage magnitude is less than the different reference voltage magnitude,  
transferring the different signal with the third voltage magnitude to the second  
node; and  
if the third voltage magnitude is greater than the different reference voltage magnitude,  
reducing the first voltage magnitude to a fourth voltage magnitude less than or  
equal to the reference voltage magnitude; and  
transferring the different signal with the fourth voltage magnitude to the second  
node.